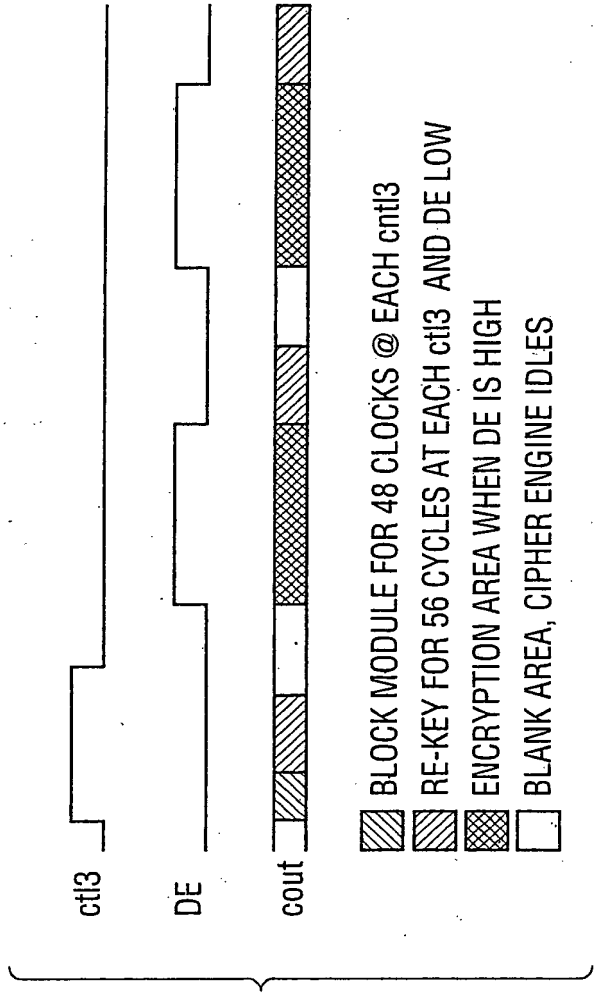
ctl3
DE
cout
BLOCK MODULE FOR 48 CLOCKS @ EACH cntl3
RE-KEY FOR 56 CYCLES AT EACH ctl3 AND DE LOW
ENCRYPTION AREA WHEN DE IS HIGH
BLANK AREA, CIPHER ENGINE IDLES

FIG. 1
(PRIOR ART)

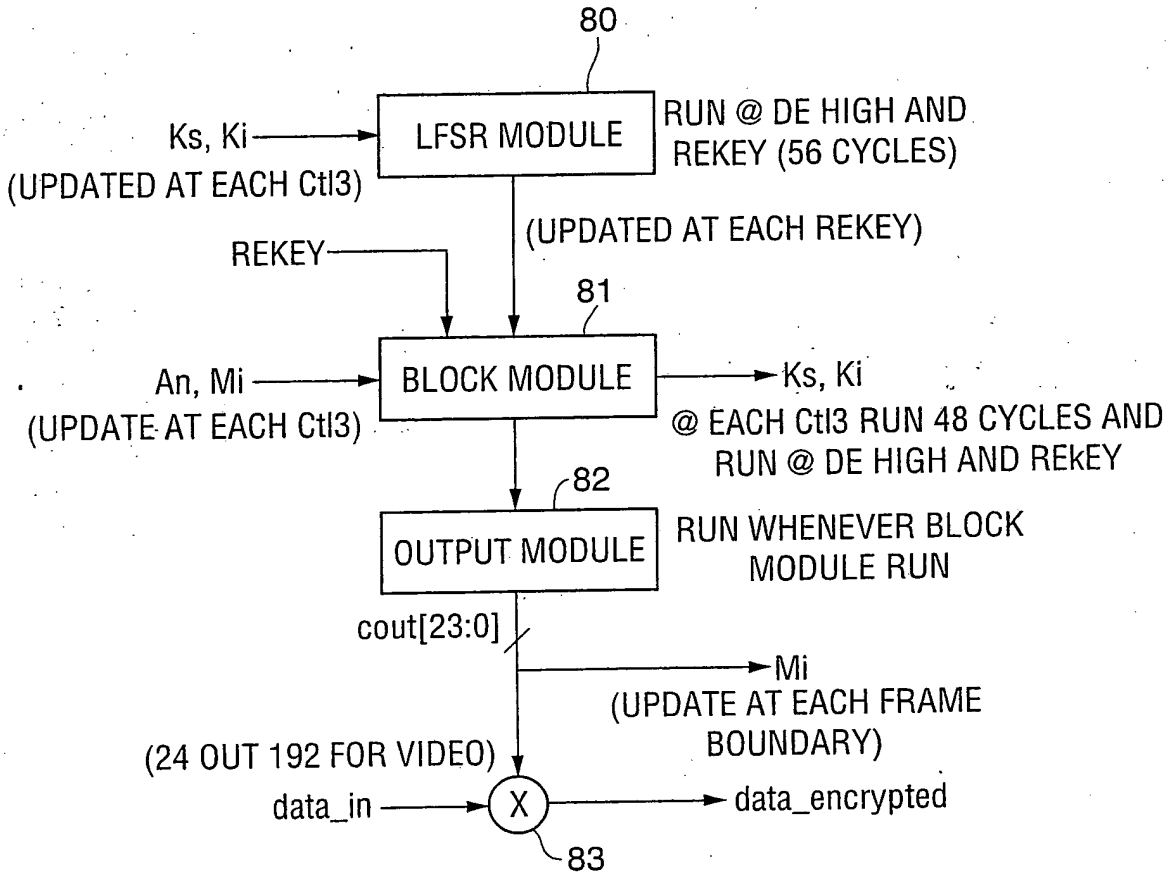

FIG. 2
(PRIOR ART)

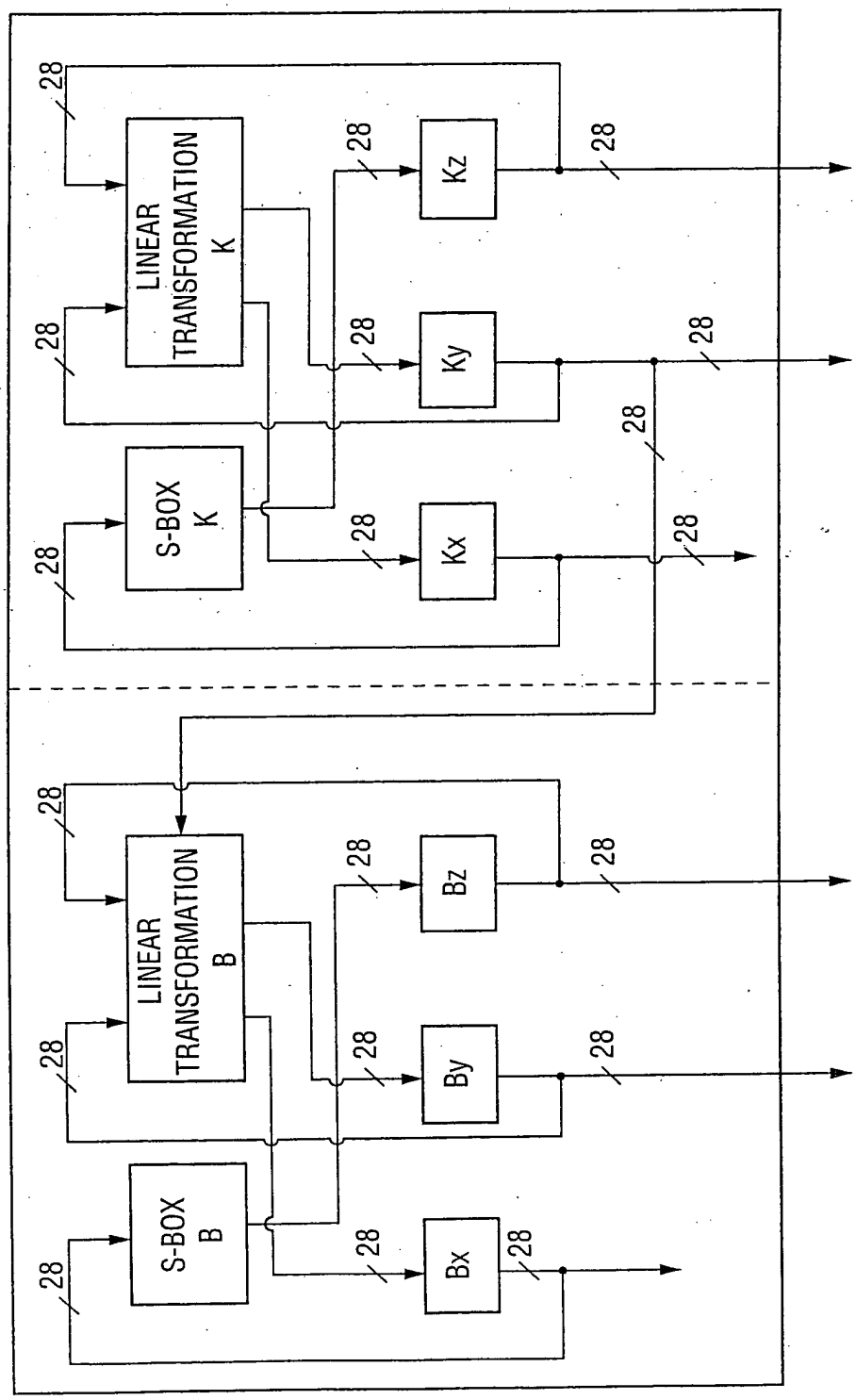

FIG. 3
(PRIOR ART)

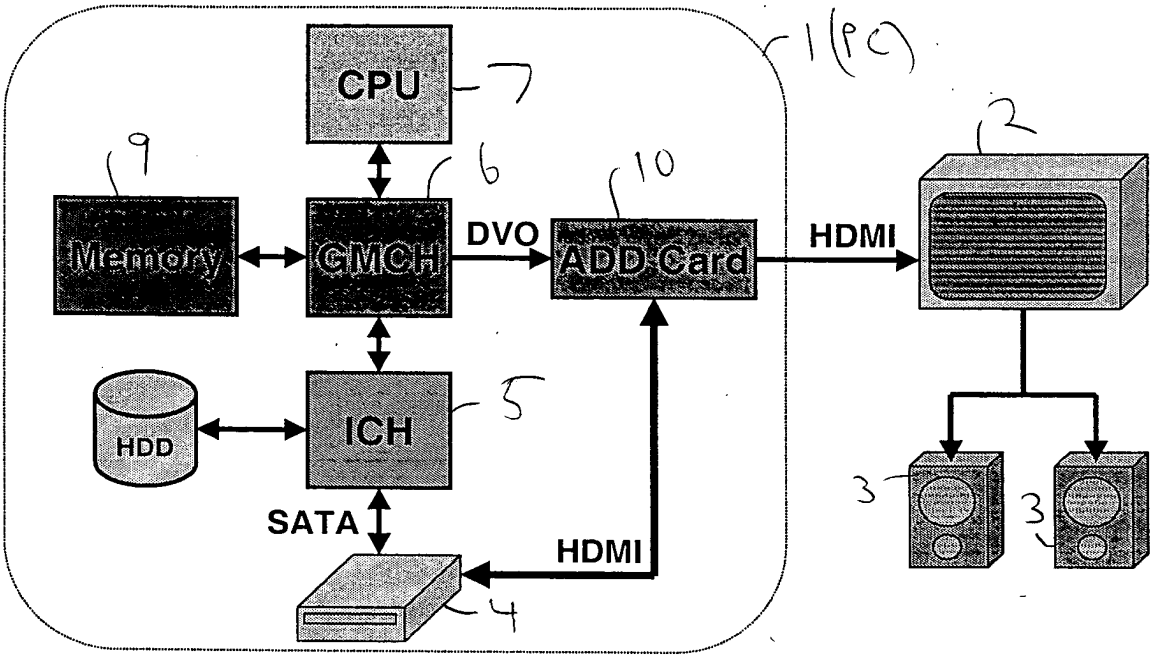
1(PC)
CPU
7
9
6
10
Memory
GMCH
DVO
ADD Card
HDMI
2
HDD
ICH
5
3
3
SATA
HDMI
4

FIG. 4

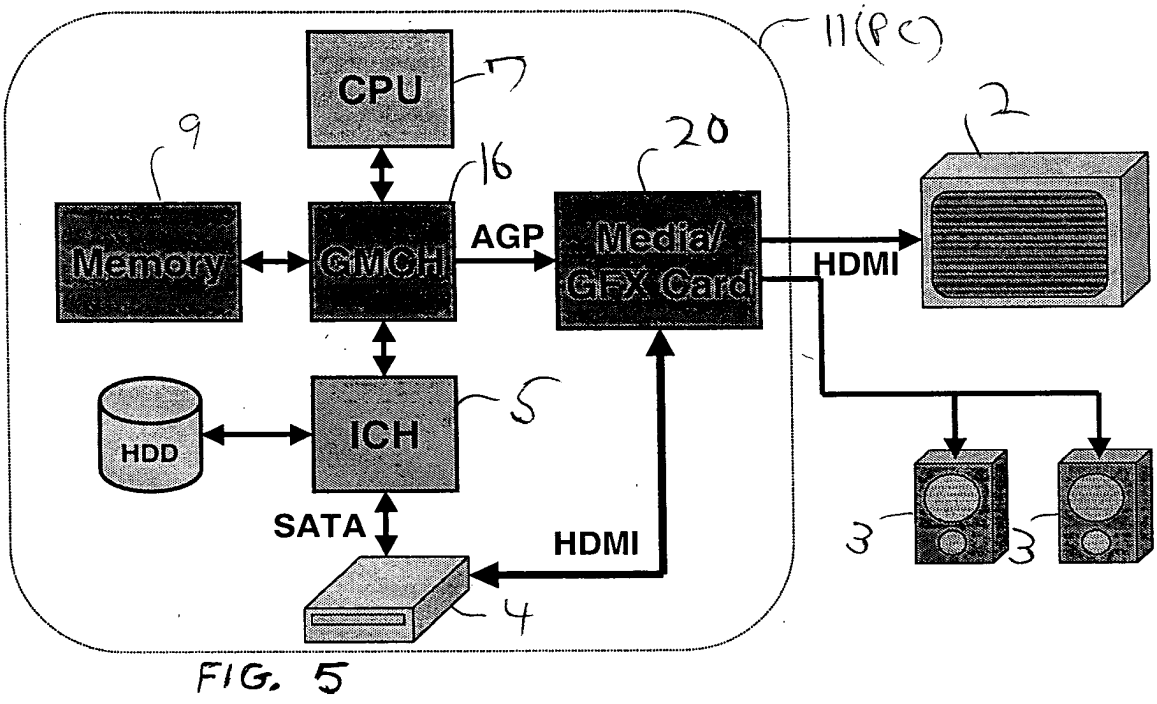
11(PC)
CPU
7
9
16
20
Memory
GMCH
AGP
Media/
GFX Card
HDMI
2
HDD
ICH
5
3
3
SATA
HDMI
4

FIG. 5

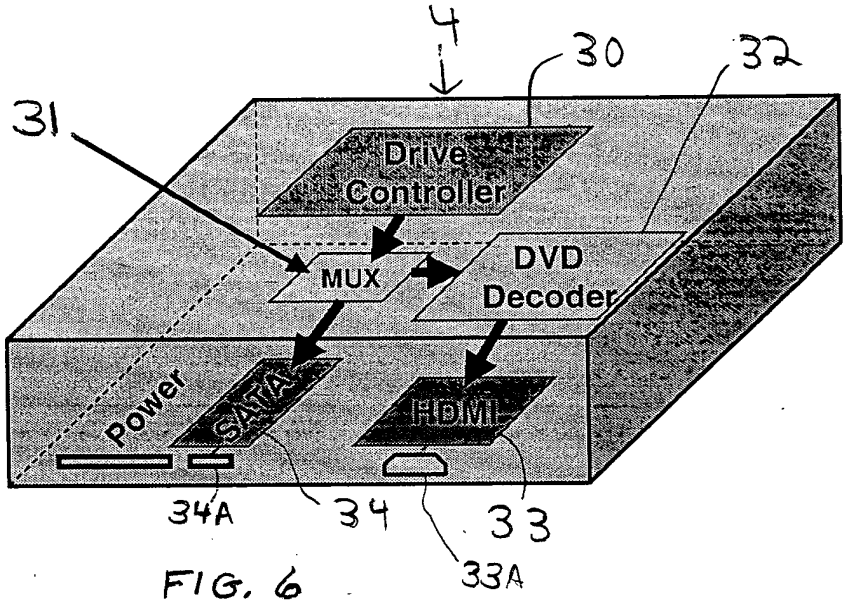
4
30
32
31
Drive Controller
MUX
DVD Decoder
Power
SATA
HDMI
34A
34
33
33A

FIG. 6

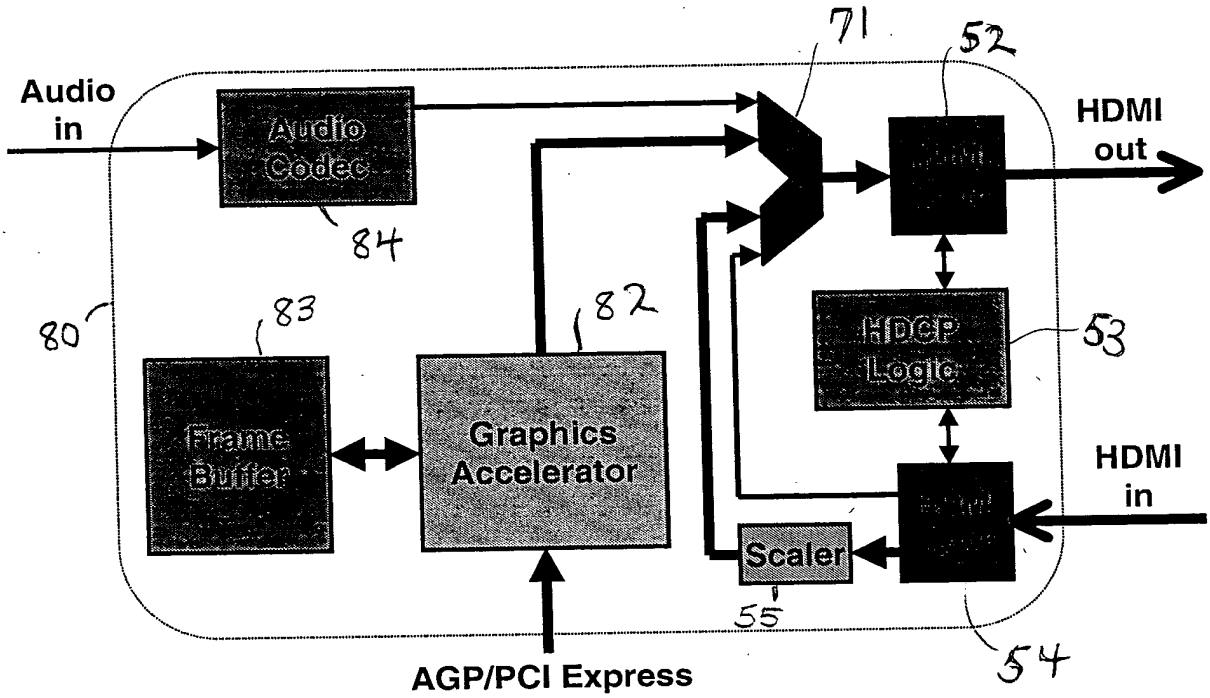
71
52
Audio in
Audio Codec
84
HDMI out
80
83
82
HDCP Logic
53
Frame Buffer
Graphics Accelerator
HDMI in
Scaler
55
54
AGP/PCI Express

FIG. 10

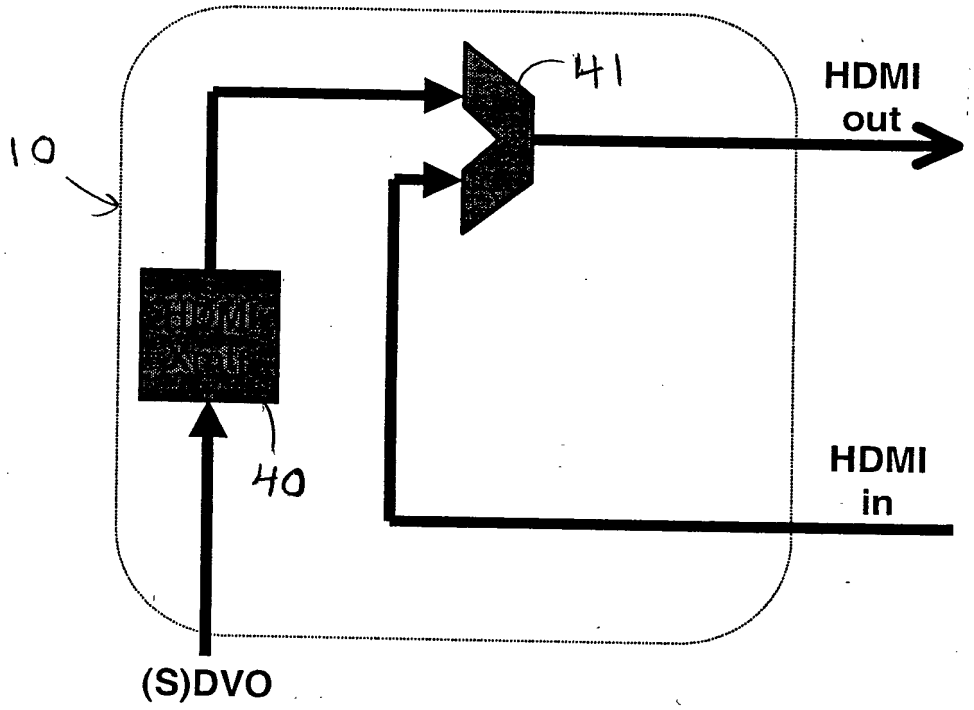
10
41
HDMI
out
HDMI
in
40
(S)DVO

FIG. 7

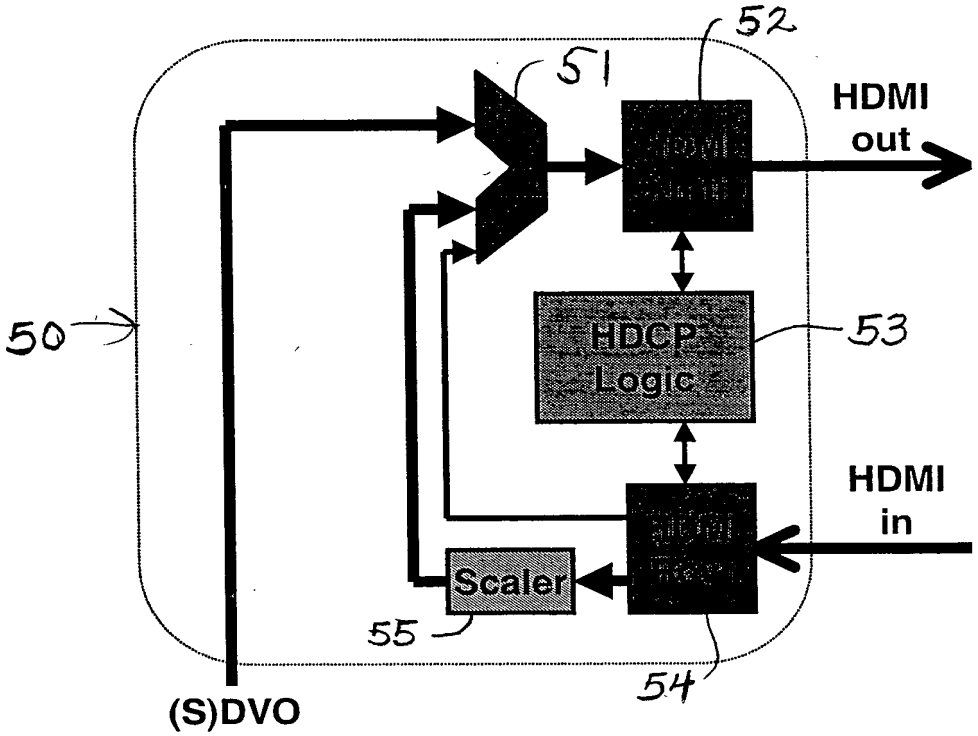
50
51
52
HDMI
out
HDCP
Logic
53
HDMI
in
Scaler
55
54
(S)DVO

FIG. 8

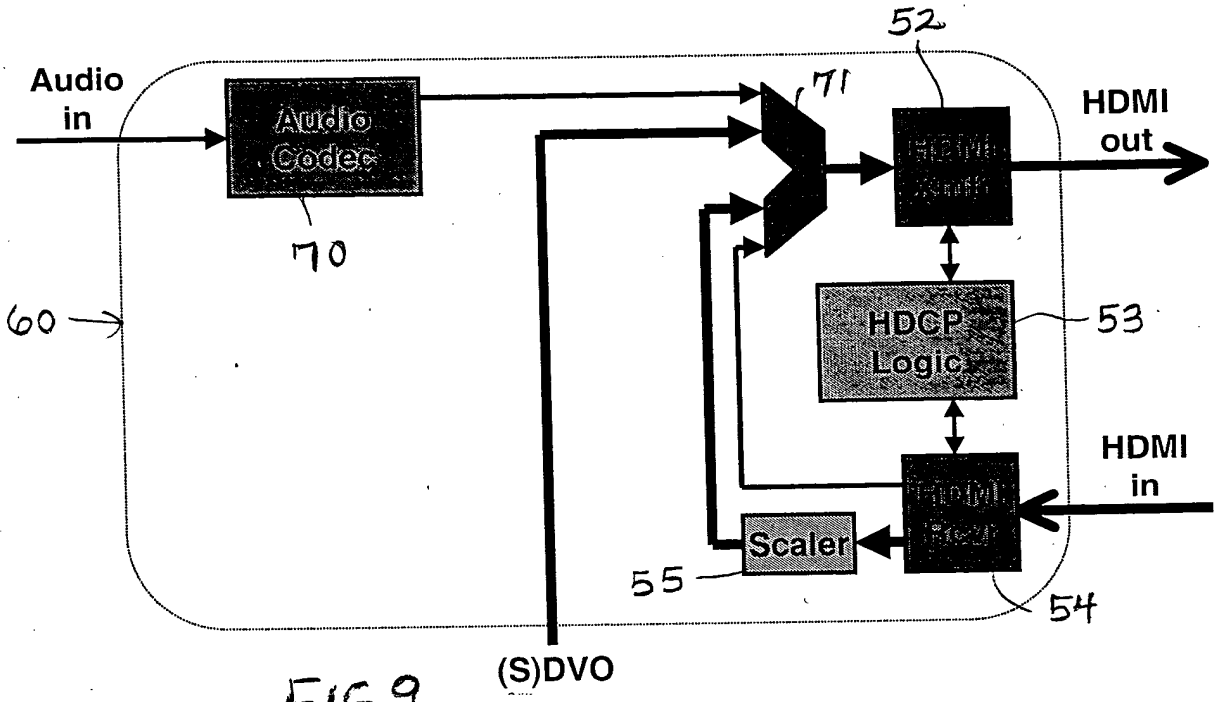
Audio in
Audio Codec
70
71
52
HDMI out
60
HDCP Logic
53
HDMI in
Scaler
55
54
(S)DVO

FIG. 9

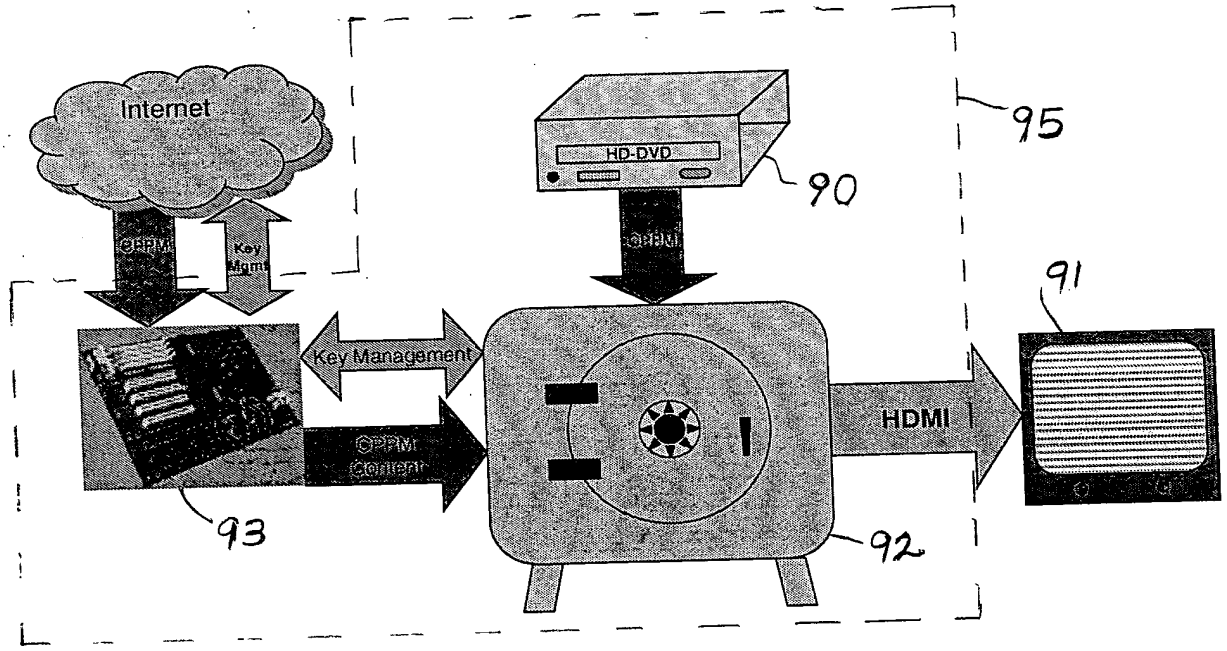
Internet
HD-DVD
90
95
91
Key Management
HDMI
93
92

FIG. 11

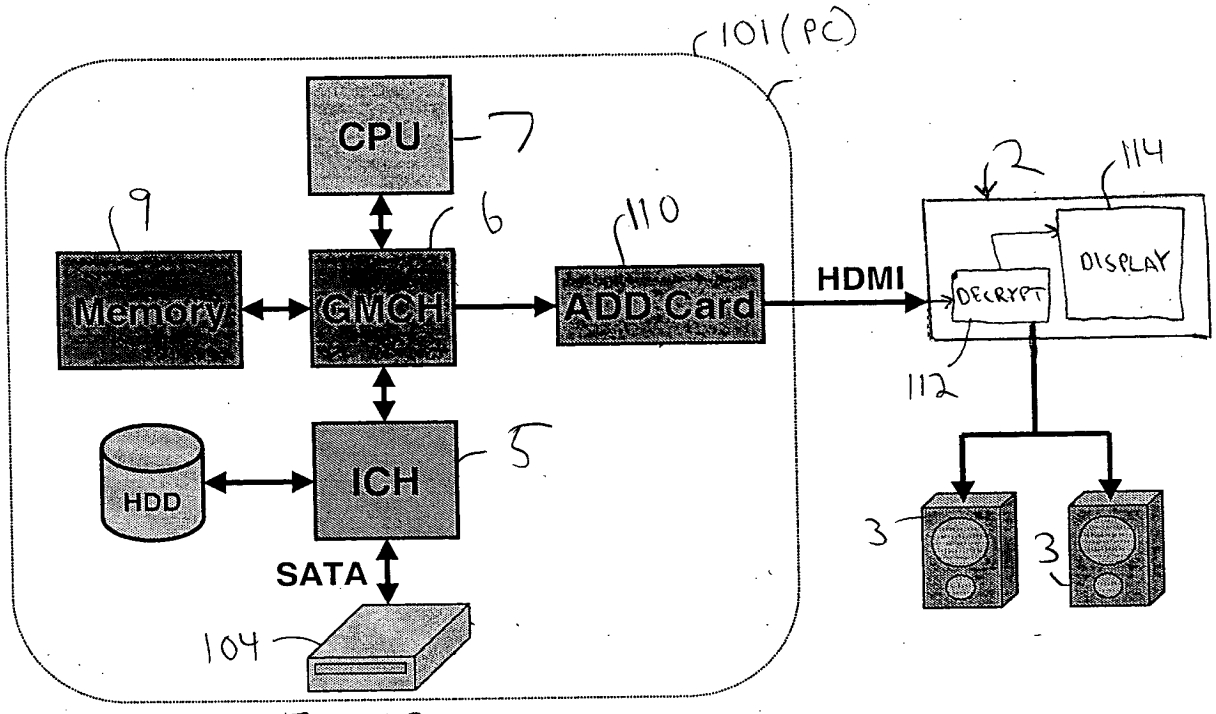
101 (PC)
CPU
7
9
6
110
Memory
GMCH
ADD Card
HDMI
2
114
DISPLAY
DECRYPT
112
HDD
ICH
5
3
3
SATA
104

FIG. 12

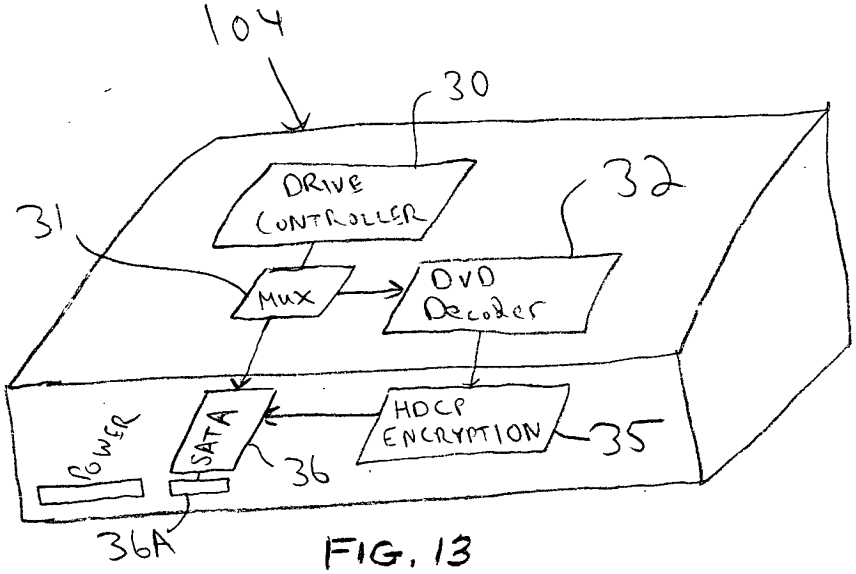
104
30
DRIVE CONTROLLER
32
31
MUX
DVD Decoder
POWER
SATA
HDCP ENCRYPTION
35
36
36A

FIG. 13